

Serial No.: 10/829,578

Examiner: S. Yam

Title: IMAGING APPARATUS WITH THREE DIMENSIONAL CIRCUIT BOARD

REMARKS/ARGUMENTS

Reconsideration is requested in view of the following remarks. Claims 1, 2 and 4 have been editorially revised. Support for the revisions to claim 1 can be found on page 5, lines 14-21 of the specification and Figures 2 and 3. Support for the revisions to claim 2 can be found on page 8, lines 2-3, page 9, lines 10-11, page 10, lines 12-13 of the specification and Figure 6. Support for the revisions to claim 4 can be found on page 7, lines 8-13 of the specification and Figures 2 and 3. Claims 1-6 remain pending in the application.

Claim Rejections – 35 USC §103

Claims 1, 2 and 4 are rejected under 35 U.S.C. §103(a) as unpatentable over Shinomiya (US Pre-grant Publication No. 2001/0055073). Applicant respectfully traverses this rejection.

The claimed imaging apparatus requires 1) a wiring pattern formed on the surface of the bottom portion of the three-dimensional circuit board opposite to the barrel portion, 2) the semiconductor imaging device to be mounted on the wiring pattern formed on the surface of the bottom portion of the three-dimensional circuit board opposite to the barrel portion, and 3) the semiconductor imaging device to be bare-mounted.

The claimed imaging apparatus remedies the following problems relating to conventional imaging apparatus such as that disclosed by Shinomiya. In conventional imaging apparatus, for example, the imaging light is deteriorated; or the OB (optical black), which is a black reference optical standard, varies due to light entering the bare-mounted semiconductor imaging device from a surface opposite to a light-receiving surface, which prevents acquisition of an excellent imaging signal. Thickness reductions of the semiconductor imaging device have therefore been limited, which poses obstacles to the thickness reduction of the imaging apparatus as described, for example, on page 1, lines 23-32 of the specification.

The claimed imaging apparatus however includes sufficient shielding characteristics in the region of the flexible printed circuit, disposed on the three-dimensional circuit board on the side opposite to the barrel portion, facing the

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semiconductor imaging device, and thus remedies the foregoing problems associated with conventional imaging apparatus such as that disclosed by Shinomiya.

Further, a three-dimensional circuit board including a fixing cap (corresponding to the "barrel-portion" in the claimed invention) 105 and a fixing pedestal (corresponding to the "bottom portion" in the claimed invention) 104 is provided on a printed circuit rigid board 101 as shown in Figure 13 of Shinomiya. A solid state imaging element 109 is mounted on a surface of the board 101 on the side of the fixing pedestal 104.

It is clear from Figure 13 that the solid state imaging element 109 is mounted by wire bonding. Shinomiya thus fails to disclose or suggest that the semiconductor imaging device is bare-mounted as recited in claim 1.

Further, although not clearly mentioned by Shinomiya, any person having ordinary skill in the art would recognize from Figure 13 that a wiring pattern is formed on a surface of the board 101 on which the solid state imaging element 109 is mounted (an upper surface). Shinomiya however, neither discloses nor suggests that the wiring pattern is formed on the surface of the fixing pedestal 104 opposite to the fixing cap 105. Further, it is clear from Figure 13 that the solid state imaging element 109 is mounted not on the fixing pedestal 104, but instead on the board 101. Shinomiya thus fails to disclose or suggest either a wiring pattern formed on the surface of the bottom portion of the three-dimensional circuit board opposite to the barrel portion as recited in claim 1, or the semiconductor imaging device mounted on the wiring pattern formed on the surface of the bottom portion of the three-dimensional circuit board opposite to the barrel portion as recited in claim 1.

The rejection also asserts that the fixing pedestal 104 and the board 101 of Shinomiya correspond to the "barrel portion" and the "bottom portion" of the claimed invention respectively. In view of the foregoing, this is not a reasonable interpretation. Regardless, Shinomiya fails to disclose or teach that the wiring pattern is formed on the surface of the board 101 opposite to the fixing pedestal 104 (the surface in contact with a flexible board 201); and the solid state imaging element 109 is not mounted on this surface. Shinomiya thus fails to disclose or teach that a wiring pattern is formed on the surface of the bottom portion of the three-dimensional circuit board opposite to the barrel portion as recited in claim 1, or that the semiconductor imaging device is mounted on the

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wiring pattern formed on the surface of the bottom portion of the three-dimensional circuit board opposite to the barrel portion as recited in claim 1.

For at least these reasons, claim 1 is patentable over Shinomiya. Applicant does not concede the correctness of the rejections. Claims 2 and 4 are also patentable over Shinomiya since they depend from claim 1 that is allowable.

Further, Shinomiya fails to disclose or teach that the thickness of the semiconductor imaging device is reduced to 0.3 mm or smaller as recited in claim 2. When attempting to achieve a thinner imaging apparatus including the limitations recited in claim 1, it is conceivable that the back surface (the surface opposite to the wiring pattern) of the semiconductor imaging device is ground so as to reduce the thickness of the semiconductor imaging device. Figure 6 of the specification illustrates that even when the semiconductor imaging device has a thickness of 0.3 mm as recited in claim 2, the image quality does not deteriorate in a bright environment. Shinomiya fails to disclose or teach such a semiconductor imaging device. For at least these reasons, claim 2 is further patentable over Shinomiya. Applicant does not concede the correctness of the rejection.

The rejection also asserts that "a flexible printed circuit inherently contains ... metal foil contacts laminated on the surface of the flexible printed circuit on the side facing attached electronic components for conveying the electrical signals."

In contrast, the metal foil as recited in claim 4 is laminated on the flexible printed circuit... on a surface opposite to a surface facing the semiconductor imaging device." The metal foil as recited in claim 4 is thus different from the metal foil contacts described in the rejection.

Further, the metal foil as recited in claim 4 is laminated entirely on the region of the flexible printed circuit. The metal foil of claim 4 is therefore not a plurality of fine wirings that are usually formed on the flexible printed circuit for conveying the electrical signals. The metal foil of claim 4 is thus different from the metal foil contacts described in the rejection. Shinomiya therefore neither discloses nor teaches the limitations recited in claim 4. For at least these reasons, claim 4 is further patentable over Shinomiya. Applicant does not concede the correctness of the rejection.

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Claim 3 is rejected under 35 U.S.C. §103(a) as unpatentable over Shinomiya in view of Nakagishi et al. (US 2001/0010562). Applicant respectfully traverses this rejection for the same reasons discussed above regarding the rejection of claim 1. Claim 3 is also patentable since it depends from claim 1 that is allowable.

Further, Nakagishi discloses an infrared cutting filter as a constituent element of an optical unit (paragraph [003] of Nakagishi). This optical filter is disposed on the side of a subject with respect to the semiconductor imaging device.

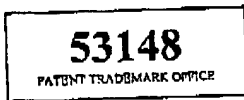
In contrast, the flexible printed circuit entirely covers a surface of the semiconductor imaging device opposite to a surface thereof facing the optical system, as recited in claim 1. The claimed flexible printed circuit therefore is disposed on the side opposite to the subject with respect to the semiconductor imaging device.

Further, claim 3 recites that in the region of the flexible printed circuit facing the semiconductor imaging device, the shielding characteristics against light with a wavelength longer than a visible range is higher than that against light in the visible range. The infrared cutting filter disposed on the side of the subject with respect to the semiconductor imaging device disclosed by Nakagishi neither discloses nor suggests the features of claim 3. For at least these reasons, claim 3 is further allowable over the cited art, alone or in combination. Applicant does not concede the correctness of the rejection.

Claims 5 and 6 are rejected under 35 U.S.C. §103(a) as unpatentable over Shinomiya in view of Gillete et al. (US 5,742, 484). Applicant respectfully traverses the rejections for the same reasons discussed above regarding the rejections of claims 1 and 4. Claims 5 and 6 are also patentable since they depend ultimately from claim 1 that is allowable. Applicant does not concede the correctness of the rejections.

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Favorable reconsideration in the form of a Notice of Allowance is requested. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone Applicant's primary attorney-of-record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.



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Respectfully submitted,

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